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Docket No. 10017911-3-Streeter (1509-240A) PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	
Inventors: Kenneth KOCH II et al.	:
	:
U.S. Patent Application No. 10/777,174	: Group Art Unit: 2816
:	
Filed: February 13, 2004	: Examiner: Long T. NGUYEN
:	
For: DRIVER CIRCUIT CONNECTED TO PULSE SHAPING CIRCUITRY	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attn: BOARD OF PATENT APPEALS AND INTERFERENCES

AMENDED BRIEF ON APPEAL

Further to the Notice of Appeal filed July 6, 2005, and Notice of Non-Compliant Appeal Brief mailed December 1, 2005 (per PAIR), in connection with the above-identified application on appeal, herewith is Appellant's Amended Brief on Appeal. The $500 Appeal Brief fee was paid on September 6, 2005.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25.

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TABLE OF AUTHORITIES

Cases

I. Real Party in Interest

The real party in interest is Hewlett-Packard Development Company, L.P., a Texas limited partnership.

II. Related Appeals and Interferences

There are no related appeals and/or interferences.

III. Status of Claims

Claims 14, 16-18 and 20-24 are allowed.

Claims 2, 4-6, 13, 15 and 19 are cancelled.

Claims 1, 3, 7-12, 25 and 26 are rejected, with claims 1, 3, 7-11 and 25-26 being rejected under 35 U.S.C. 102(b) as being anticipated by Love (USP 5,068,553), and claims 1, 3, 7-12 and 25 being rejected under 35 U.S.C. 103(a) as being unpatentable over Hamasaki et al. (USP 5,694,065) in view of Rapp (USP 5,280,420).

IV. Status of Amendments

The only amendment, dated June 3, 2005, after Final Rejection was entered. This amendment does not involve the present appeal because it combines claim 24, indicated as containing allowable subject matter in the Final Rejection, with the claim upon which claim 24 depends.

V. Summary of Claimed Subject Matter

The invention concerns shaping circuitry 10 for causing the source drain paths of P channel field effect transistor (PFET) 48 and N channel field effect transistor (NFET) 50 to be respectively on and off while the voltage of source 12 connected to terminal 39 has a first level, and off and on while the voltage source has a second level (¶1). The source drain paths of PFET 48 and NFET

50 are connected in series across opposite DC power supply terminals, in the form of terminal 16, connected to the positive DC power supply voltage + V_{DD} at terminal 16, and ground terminal 18 (¶22). The pulse shaping circuitry prevents the source drain paths of both PFET 48 and NFET 50 from being on simultaneously to prevent excessive current flow between terminals 16 and 18 (¶¶1, 24).

Claim 1, upon which all remaining rejected claims depend, can be read on the pulse shaping circuitry in two different ways, both of which are described in this portion of the Brief. The pulse shaping circuitry can, in one arrangement, be considered as including inverter 20 and capacitor 32 that is formed by dielectric between the gate and the common source and drain electrodes of NFET 52 (¶¶19, 23). In such an interpretation, PFET 48 must be interpreted to be the first transistor of claim 1, while NFET 50 must be considered to be the second transistor of the claim. Capacitor 32 is connected between the gate of PFET 48 (i.e., the first transistor) and ground terminal 18 (¶¶11, 22). Inverter 20 includes a resistor 40 that supplies current to capacitor 32 and the gate of PFET 40 while NFET 38 of the inverter is on, as a result of the voltage of source 12 at terminal 39 having a high value (¶20). Under this scenario, ground terminal 18 (¶18) must be the first power supply terminal and terminal 16, connected to + V_{DD} (¶18) must be the second power supply terminal and PFET 48, which has a conductivity type opposite to the conductivity type of NFET 52 that forms capacitor 32, must be the "one" of the transistors, while NFET 50 is the "other" of the transistors. In response to the voltage of source 12 at terminal 39 having a high value, NFET 38 is on, causing current to flow from capacitor 32 through resistor 40 and NFET 38 back to capacitor 32 via ground terminal 32. While current is thus being supplied to capacitor 32 (formed by NFET 52) and the gate of PFET 48, NFET

transistor 50 is on and current is supplied to NFET 50 by the grounded power supply terminal 18 (¶29).

In the second scenario, the pulse shaping circuitry includes inverter 22 (¶21) and capacitor 34 (¶19) that is formed by PFET 54 (¶23) so the "one" transistor must be NFET 50, while the "other" transistor must be PFET 48. Capacitor 34 is thus connected between the gate of the "one" transistor, formed by NFET 50, and the positive power supply voltage at terminal 16 (¶23). In response to the voltage of source 12 at terminal 39 having a low voltage, PFET 42 of inverter 22 is on, causing current to flow from the positive power supply voltage at terminal 16 through resistor 46 to capacitor 34 formed by PFET 54 and to the gate of NFET 50. While current is flowing through resistor 46 to capacitor 34 and the gate of NFET 50, the source drain path of PFET 48 (the "other" transistor for this scenario) is on, causing current to flow from the positive voltage at terminal 16 (the first power supply terminal for this scenario) (¶27).

Waveform 62 of Figure 2 indicates PFET 48 is off while the voltage of source 12 at terminal 39 is low, as well as during the initial portion of the period while the voltage of source 12 at terminal 39 is high. In response to the negative going transition 68 of source 12, PFET 48 is switched from the on to the off condition. Waveform 63 of Figure 2 indicates NFET 50 goes from an off to an on state in response to the positive going transition 80 of source 12. NFET 50 stays in the off state during the entire time while source 12 has a positive voltage and for the initial portion of the period after transition 68, at which time NFET 50 switches from an off to an on state. NFET 50 goes from an off to an on state in response to the voltage across capacitor 32, indicated by waveform portion 74, crossing a threshold point 72. NFET 50 goes from the on to the off state in response to the positive going transition 80 of source 12, which causes the

immediate discharge of capacitor 34 through NFET transistor 44 to ground terminal 18 (¶¶28, 32).

Similar operation occurs during the half cycles of source 12 while the source is deriving a high output voltage. PFET 48 turns on in response to the voltage across the source gate electrodes thereof crossing the threshold of PFET 48. Turn on of PFET 48 is subsequent to the positive going transition 80 of source 12, but is after the turn off of NFET 50 (¶33). Consequently, PFET 48 and NFET 50 are not both on simultaneously to minimize power consumption and prevent the flow of crowbar current from the power supply (¶24). Because crowbar current cannot flow, the likelihood of overheating of the integrated circuit chip including the circuit is obviated for this purpose (¶5).

VI. Grounds of Rejection to be Reviewed on Appeal

A. Love does not anticipate claims 1, 3, 7-11, 25 or 26

B. Hamasaki et al., in combination with Rapp, Does Not Render the Subject Matter of Claims 1, 3, 7-12 and 25 Obvious

VII. Argument

A. Love Does Not Anticipate Claims 1, 3, 7-11, 25 and 26

The rejection of claims 1, 3, 7-11, 25 and 26 as being anticipated by Love, USP 5,068,553, is wrong. Claim 1, upon which claims 3, 7-11, 25 and 26 depend, either directly or indirectly, distinguishes over Love by requiring (1) the first power supply terminal to be connected for supplying current to the source drain path of the "other" of said transistors while the source drain path of the "other" of said transistors is on, (2) the capacitor to be a field effect device having a conductivity type opposite to the conductivity type of said "one" of said transistors, and (3) the capacitor to be connected across the gate electrode said "one" of said

transistors and the first power supply terminal. This language means that if the "one" transistor of the claim is the PFET transistor of the claim, the conductivity type of the transistor that forms the capacitor is an NFET; if the one transistor of the claim is an NFET the transistor that forms the capacitor is a PFET.

The Final Rejection does not appear to properly interpret the words "one" and "other." The word "one" can refer to either the PFET or NFET set forth in line 4. If the word "one" refers to the PFET mentioned in line 4, the word "other" refers to the NFET in line 4. In contrast, if the word "one" is interpreted as the NFET set forth in line 4, the word "other" refers to the PFET of line 4. This interpretation is necessary because of the use in claim 1 of the clauses "the gate electrode of one of said transistors" and "the other of said transistors."

In Love, the grounded power supply terminal supplies current to NFET 88 while NFET 88 is on and V_{DD} supplies current to PFET 86 while PFET 86 is on. MOSFET capacitor 80 (correctly identified in the Final Rejection as an NFET) is connected between the gates of PFET 86 and NFET 88 and ground.

If ground of Love is considered to be the first power supply terminal of appellants' claim 1, the "other" transistor of claim 1 must be considered as NFET 88 of Love. However, NFET 88 of Love has the same conductivity type as NFET 80 of Love that forms the capacitor between the gate of NFET 88 and ground. Hence, the interpretation of Love in this paragraph is not consistent with claim 1.

If V_{DD} of Love is considered the first power supply terminal of appellants' claim 1, the "other" of said transistors of claim 1 must be considered as PFET 86 of Love. While PFET 86 of Love has a conductivity type opposite to that of NFET 80 that forms a capacitor, NFET 80 is

not connected between the gate of PFET 86 and the first power supply terminal, V_{DD}. Instead NFET 80 is connected between the gate of PFET 86 and ground, that is opposite from the first power supply terminal V_{DD}. As a result, the interpretation of Love in this paragraph is also inconsistent with claim 1.

The Final Rejection, in attempting to apply Love, fails to discuss the connections of the power supply terminals to PFET 86 or NFETs 80 and 88. Hence, the Final Rejection does not establish a prima facie case of anticipation. There is no rebuttal in the record to appellants' application of the language of claim 1 to Love. Consequently, the rejection of claim 1 as being anticipated by Love is incorrect.

Appellants also cannot agree with the statement in the Final Rejection that the Figure 3 circuit of Love is such that the pulse shaping circuit including PFET 68, NFET 70 and resistive element 72 necessarily prevents both source-drain paths of PFET 86 and NFET 88 from being on simultaneously. As noted in paragraphs 4 and 5 of the "Background Art" portion of the present application, a problem of prior art drivers including first and second opposite conductivity type transistors, such as PFET 86 and NFET 88 of Love, is that both transistors have a tendency to be on simultaneously during switching between first and second levels of an input source. Since the Examiner is apparently relying on inherency for this feature, he must prove that the Love circuit necessarily causes PFET 86 and NFET 88 to be such that the source drain paths thereof are prevented from being on simultaneously.

The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993); In re Oelrich, 666 F.2d 578, 581-82, 212

USPQ 323, 326 (CCPA 1981). To establish inherency, extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference and that it would be so recognized by persons of ordinary skill in the art. Inherency may not be established by possibilities or probabilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient. In re Roberston, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999). In relying upon a theory of inherency, the Examiner must provide a basis in fact or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the prior art. Ex parte Levy, 17 USPQ2d 1461, 1464 (BPAI 1990). Since the Examiner has not provided a rationale or evidence to show that Love inherently prevents the source drain paths of PFET 86 and NFET 88 from being on simultaneously, the rejection of claims 1, 3, 7-11 and 25-26 based on Love is incorrect and must be withdrawn.

The Final Rejection, in analyzing Love, concludes that because PFET 86 and NFET 88 of Love have opposite conductivity, the PFET and NFET cannot be on simultaneously. However, such a statement flies in the face of the statements set forth in the Background portion of appellants' application, at paragraphs 5-7. The first and second paragraphs of the Background art of appellants' application (i.e., paragraphs 2 and 3) describe a circuit of the type disclosed by Love that includes PFET 86 and NFET 88. There is no rationale provided by the Examiner that PFET 86 and NFET 88 will not be on simultaneously. The Background of the Invention segment of Love in column 2, lines 14-23, indicates that Love is interested in providing delay stages that work quickly at low V_{DD}, i.e., low power supply voltage levels, as well as at high power supply levels. These statements make it incumbent upon the Examiner to provide rationale or evidence to support his position that PFET 86 and NFET 88 of Love are

not simultaneously on during a transition of the voltage at terminal 62. Because the Examiner has failed to provide such rationale or evidence, the anticipation rejection of claim 1 based on Love is wrong.

Claims 3, 7-11, 25 and 26 are not anticipated by Love because they depend on claim 1.

B. The Hamasaki Reference

Hamasaki et al. discloses a circuit wherein the source drain paths of PFET transistor 50 and NFET transistor 60 are connected between a positive power supply voltage at terminal 30 and a ground terminal 40. An input signal at terminal 10 is applied in parallel to inverters IV 1 and IV 2, respectively having an output terminal connected to variable delay circuits 70 and 80. Delay circuit 70 includes a series resistor R_n and shunt capacitor C_n, one terminal of which is connected to ground terminal 46. The junction between the resistor and capacitor of variable delay circuit 70 is connected to the gate of PFET 50, having a source electrode connected to terminal 30. Variable delay circuit 80 includes series resistor R_p and shunt capacitor C_p. Capacitor C_p is connected between the gate of NFET 60 and ground terminal 48.

Capacitors C_n and C_p are both formed in the same manner. As such, each of the capacitors includes a silicon substrate 702, a power supply metal conductor 704 maintained at the power supply voltages at nodes 30 and 32, a serpentine metallic layer 700 that forms the electrode of the capacitor connected to the gate of PFET 50 (for capacitor C_n) and the gate of NFET 60 (for the capacitor C_p). In addition each of capacitors C_n and C_p includes a pair of insulating layers 708 and 710, and a silicon substrate 702 that is at the power supply voltage. Metal conductor 706 is at ground potential in capacitor C_n and capacitor C_p.

The portion of Hamasaki et al. dealing with capacitor C_p is not germane to claim 1 for the same reasons discussed supra, in connection with Love. This is because capacitor C_p has one electrode thereof at ground potential, the same potential to which the source electrode of NFET 60 is connected. In appellants' circuit, as defined by claim 1, such a connection cannot exist, as described supra, in connection with the rejection based on Love. Appellants' claim 1 precludes such a connection because the capacitor is required to be connected across the gate electrode of one of said transistors and a first of the power supply terminals that supplies current to the source drain path of the other of the transistors while the source drain path of the other of the transistors is on. As described in connection with the Summary of Claimed Subject Matter portion of this Brief, these connections, as applied to Hamasaki et al., must be interpreted as the connection of capacitor 34 between the gate of NFET 50 and the positive power supply at terminal 16 or the connection of capacitor 32 between the gate of PFET 48 and ground.

In Hamasaki et al., capacitor C_p does not meet these requirements of claim 1. This is because capacitor C_p is connected between the gate of NFET 60 and ground and because of the connection of the source of NFET 60 to ground. This is the basis for the statement in paragraph 3 of the Koch Declaration, which states: "Replacing capacitor C_p with a P channel field effect transistor that functions as a capacitor is not appropriate because the P channel field effect transistor of my circuit is connected between the gate of the N channel transistor and the power supply terminal."

Based on the foregoing, the only remaining issue with regard to claim 1 and the rejection based on Hamasaki et al. and Rapp concerns the obviousness of replacing capacitor

C_p of Hamasaki et al. with an NFET transistor that is connected as capacitor as disclosed by Rapp.

C. The Koch Declaration Overcomes the Obviousness Rejection based on Hamasaki and Rapp

The Final Rejection states it would have been obvious to have replaced capacitor C_n of Hamasaki with a field effect device having a conductivity opposite to the conductivity type of PFET 50, as disclosed by Rapp. The Final Rejection correctly states that Rapp discloses a capacitor formed as an MOS transistor having its source and its drain connected together. The Final Rejection then states it would have been obvious to have replaced capacitor C_n of Hamasaki et al. with the device Rapp discloses, because such a substitution would result in more efficient implementation in silicon so that "the operation of the circuitry would be more efficiency [sic] since the circuit is fully integrated."

Appellants have rebutted the foregoing position set forth in the Final Rejection by submitting evidence as to why one of ordinary skill in the art would not have made the substitution the Examiner states would have been obvious. Appellants have submitted the Declaration of Kenneth Koch II, who is considered by his employer, Hewlett-Packard Company, to be an expert in the field of electronic circuitry. Mr. Koch has testified, under penalty of perjury, about numerous disadvantages associated with replacing the capacitor illustrated in Figures 4 and 5 of Hamasaki et al. with a field effect device.

Paragraph 4 of Mr. Koch's declaration states that, if possible, designers of electronic circuits generally avoid the use of field effect transistor devices that are connected in the capacitance mode. This is because field effect transistors connected in the capacitance mode have

significant channel and diffusion resistance. The channel and diffusion resistance is usually in the thousands of ohms/square range, which results in the field effect transistor not behaving like a capacitor at higher frequencies. The value of the channel and diffusion resistance is usually poorly controlled by manufacturers of integrated circuits.

A further disadvantage of using field effect transistor devices as capacitors is that the field effect transistor gate to channel capacity is a function of the gate to channel voltage, resulting in a capacitor with a capacitance that may be difficult to control. To obtain the maximum capacitance per unit area, the field effect transistor must be biased to an on state.

A further disadvantage in using field effect transistors as capacitors is the leakage current through the gate of the field effect transistor. When a field effect transistor connected in the capacitor mode is biased in the linear or saturation region, the gate leakage current, i.e., the current that leaks from the gate electrode to the channel, can be large enough to affect the performance of the circuit in an adverse manner. The gate leakage current also is a concern because many manufacturers do not provide a field effect transistor model which accurately indicates gate leakage current, if they indicate it at all. Without an accurate indication of gate leakage current, the designer is likely to make poor choices. In addition, a discrete capacitor, such as the capacitor disclosed in Figures 4 and 5 of the Hamasaki et al. reference, functions as a capacitor to a much greater extent than a field effect transistor that is connected in a capacitor mode.

Mr. Koch has testified that an N channel field effect transistor that functions as a capacitor was used in his circuit in connection with the gate of a P channel transistor and ground because of the capability of such a transistor achieving desirable switching effects. These switching effects can be achieved in a very simple manner by using such an N channel field effect transistor,

connected in a capacitor mode. As a result of the realization of the switching characteristics of the N channel field effect transistor in the capacitor mode, the normal disadvantages associated with replacing a conventional capacitor with an N channel field effect transistor are overcome for many engineering purposes.

The Examiner appears to agree with the foregoing statements because the final Office Action has not attacked the foregoing rationale set forth in the Koch Declaration. Instead, the Advisory Action attacks the Koch Declaration as being applicable only to replacing capacitor C_n of Hamasaki et al. with an N channel device. The Examiner has not, apparently, appreciated the fact that the language of claim 1 precludes replacing capacitor C_p of Hamasaki et al. with a PFET device connected in the capacitance mode.

The rejections of claims 3, 7-12 and 25 as being obvious as a result of Hamasaki et al. in view of Rapp are incorrect because each of these claims depends upon claim 1, which has been demonstrated to be unobvious over the combination of Hamasaki et al. and Rapp. In addition, claims 10, 11, 12, 25 and 26 include features not found in either Hamasaki et al. or Rapp.

Claim 10 requires the resistor to be included in the inverter and claim 12 requires the resistor to be connected between the source drain path of the NFET of the inverter and the output terminal of the inverter. In Hamasaki et al. neither resistor R_n nor resistor R_p has such a connection because neither resistor R_n nor resistor R_p can be considered as being in inverter IV 1 or inverter IV 2. The output terminal of inverter IV 1 is between the source drain paths of PFET 72 and NFET 74, while the output terminal of inverter IV 2 is between the source drain paths of inverters 82 and 84. Resistors R_n and R_p are in variable delay circuits 70 and 80. Since claims 11, 12, 25 and 26 all depend, either directly or indirectly, on claim 10, these claims are also allowable

with claim 10. In addition, claims 12 and 25 respectively require the resistor to be connected between the source drain path of the NFET of the inverter and the output terminal of the inverter. Since the resistors R_n and R_p are not included in the inverters, but are included in delay devices 70 and 80, the limitations of claims 12 and 25 are not found in Hamasaki et al.

Claim 26 requires the resistor to be connected between the source drain paths of the NFET and PFET of the inverter. The connections of the resistor to the NFET and the PFET of the inverter are such that substantial current flows through the resistor while the PFET is switched on and insubstantial current flows through the resistor while the PFET is switched on and the NFET is switched off. In contrast, when PFET 72 of the Hamasaki et al. circuit is switched on, current would appear to flow from power supply terminal 32 through the source drain path of PFET 72 to resistor R_n and capacitor C_n to ground. Similarly, when PFET 82 is switched on, substantial current would appear to flow from terminal 34 through resistor R_p and capacitor C_p to ground. While PFET 72 is on, NFET 74 would appear to be off, and while PFET 82 is on, NFET 84 would appear to be off. Hence, the foregoing requirement of claim 26 is not found in Hamasaki et al.

Clearly, Rapp does not cure the foregoing deficiencies of Hamasaki et al. vis-à-vis claims 3, 7-12, 25 and 26.

VIII. Conclusion

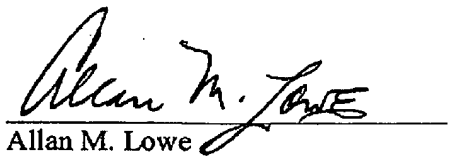
The anticipation rejection based on Love is wrong because the connections of (1) MOSFET 80 across the gate electrodes of PFET 86 and NFET 88 and (2) PFET 86 and NFET 88 to the power supply terminals do not meet the connection requirements of claim 1. The obviousness rejection of claim 1, based on Hamasaki et al. and Rapp, is incorrect because one of ordinary skill in the art would not have replaced capacitor C_n of Hamasaki et al. with an NFET

connected in the capacitor mode. Such a substitution would not have been made because of the disadvantages normally associated with such a connection, as set forth in the Koch Declaration.

Reversal of the rejections is in order.

Respectfully submitted,

Kenneth KOCH II et al.

By: 

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IX. Claims Appendix

Claim 1: A circuit comprising a first terminal for connection to a voltage source having first and second levels and a transition between the levels, a driver including first and second opposite conductivity type transistors, said first and second transistors being respectively a PFET and an NFET, each of said transistors including a gate electrode and a source drain path arranged to be switched on and off in response to a voltage applied to the gate electrode being on opposite sides of a threshold, the first and second transistor paths being connected in series across opposite power supply terminals, and pulse shaping circuitry for (a) causing the first and second source drain paths to be respectively (i) on and off while the voltage source has the first level and (ii) off and on while the voltage source has the second level, and (b) preventing both source drain paths from being on simultaneously, the pulse shaping circuitry including a resistive element and a capacitor, the resistive element being connected for supplying current to the capacitor and the gate electrode of the first transistor, the capacitor being connected across the gate electrode of one of said transistors and a first of the power supply terminals, the first power supply terminal being connected for supplying current to the source drain path of the other of said transistors while the source drain path of the other of said transistors is on, the capacitor comprising a field effect device having a conductivity type opposite to the conductivity type of said one of said transistors.

Claim 3: The circuit of claim 1 wherein said resistive element, PFET, NFET and said capacitor are included on an integrated circuit chip, and said resistive element comprises a resistor.

Claim 7: The circuit of claim 1 wherein the pulse shaping circuitry includes a switching circuit having (a) an input terminal for enabling the switching circuit to be responsive to the voltage at the first terminal and (b) an output terminal, the output terminal of the switching circuit being connected so current can flow via a DC path between (a) the first power supply terminal and (b) the capacitor and the gate electrode of said one transistor, the DC path including the resistive element.

Claim 8: The circuit of claim 7 wherein the switching circuit includes an inverter having field effect transistors.

Claim 9: The circuit of claim 8 wherein all the field effect transistors of the inverter are included on an integrated circuit chip including a resistor comprising the resistive element connected with said one field effect transistor and the inverter.

Claim 10: The circuit of claim 9 wherein the resistor is included in the inverter.

Claim 11: The circuit of claim 10 wherein the inverter includes a PFET and an NFET, the PFET and NFET of the inverter having a source drain path and a gate electrode having a connection to the first terminal so that the gate electrodes of the PFETs and NFETs of the inverter are arranged to be driven in parallel by the voltage at the first terminal, the output terminal of each of the inverters being between the source drain paths of the PFET and NFET thereof.

Claim 12: The circuit of claim 11 wherein the resistor is connected between the source drain path of the NFET of the inverter and the output terminal of the inverter.

Claim 25: The circuit of claim 11, wherein the resistor is connected between the source drain path of the PFET of the inverter and the output terminal of the inverter.

Claim 26: The circuit of claim 25, wherein the resistor is connected between the source drain paths of the NFET and PFET of the inverter, and the connection of the resistor to the NFET and PFET of the inverter is such that substantial current flows through the resistor while the PFET

is switched on and insubstantial current flows through the resistor while the PFET is switched on and the NFET is switched off.

X. Evidence Appendix

None.

XI. Related Proceedings Appendix

None.